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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,725	07/01/2003	Leonard Forbes	501268.01	5767
27073	7590	03/10/2005	EXAMINER	
LEFFERT JAY & POLGLAZE, P.A. P.O. BOX 581009 MINNEAPOLIS, MN 55458-1009			FENTY, JESSE A	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

<b>Office Action Summary</b>	<b>Application No.</b> 10/612,725	<b>Applicant(s)</b> FORBES	
	<b>Examiner</b> Jesse A. Fenty	<b>Art Unit</b> 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 December 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14, 16-18, 22, 25, 26 and 28-32 is/are rejected.
- 7) ☒ Claim(s) 15, 19-21, 23, 24 and 27 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

- a. The limitations comprising a computer system and CPU are not described in the specification such that one skilled in the art would be able to make or use the components as claimed.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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2. Claims 13, 14, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kolodny et al. (U.S. Patent No. 4,785,199).

In re claims 13 and 14, Kolodny (esp. Fig. 2) discloses a semiconductor device, comprising:

an array having memory cells for storing a desired logic state, each cell further comprising first and second adjacent FETs having respective source/drain regions (34, 36, 38, 40) and a common floating gate structure (20, 22) that is spaced apart from the source/drain regions (38, 40) of the first FET by a first distance, and spaced apart from the source/drain regions (34, 36) of the second FET by a second distance, wherein the first distance is less than the second distance;

wherein each of the respective source/drain regions further comprises a first source/drain region (conductive contacts extending upward from source/drain regions) and a spaced apart second drain region configured in a columnar structure extending upwardly from and underlying substrate, and further wherein a separation layer (insulation between the conductive contacts) is interposed between the first source/drain region and the second source/drain region.

In re claim 16, Kolodny discloses the device of claim 13, wherein the common floating gate structure is polysilicon.

In re claim 17, Kolodny discloses the device of claim 13, wherein the second distance (measured regarding the offset distance of the floating gate between 34 and 36 in proportion to the offset distance between regions 38 and 40) is about two times the first distance.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 9-12, 22, 25, 26 and 28-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama (U.S. Patent No. 4,630,085).

In re claims 1, 11, 12 and 22, Koyama (esp. Figs. 4 and 5) discloses a semiconductor device and method of forming the device, comprising:

at least one memory device, the memory device including an array having memory cells arranged in rows and columns for storing a desired logic state, each cell including a first columnar structure (29) and a spaced apart second columnar structure (30) having a floating gate (26) structure interposed between the first columnar structure and the second columnar structure and spaced apart from the first and second columnar structures, the floating gate being positioned closer to one of the first and second structures.

Koyama does not expressly disclose a CPU, keyboard, mouse, modem or external secondary mass storage device. However, it would have been obvious for one skilled in the art at the time of the invention to use the memory structure provided by Koyama in a computer system featuring such components for the purpose, for example, of using or enabling the memory device. Neither the claim nor the disclosure teaches the use of a specific CPU or other configurations for hardware devices with the claimed memory cell. Based on the disclosure of

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Koyama, and the circuit diagram of Fig. 5, those of ordinary skill in the art would be able to enable this device based on routine knowledge and experimentation.

In re claim 9, Koyama discloses the device of claim 1, further comprising an address bus ( $X_i, X_{i+1}$ ), a data bus and a control bus (C, D).

In re claim 10, Koyama discloses the device of claim 9. The use of a system controller to control the buses of claim 9 would have been obvious based on the ordinary skill of one in the art.

In re claim 25, Koyama discloses the method of claim 22, further comprising:

forming a first source/drain (22) having a first conductivity on the substrate;

forming a second source/drain region (23) proximate to the first source/drain region, the second source/drain region having the first conductivity; and

interposing a separation layer (24) between the first source/drain region (22) and the second source/drain region (23).

In re claim 26, Koyama discloses the method of claim 25, wherein forming a first source/drain region having a first conductivity comprises forming a source/drain region having an N+ conductivity (column 6, lines 37-40).

In re claim 28, Koyama discloses the method of claim 25, wherein interposing a separation layer between the first source/drain region and the second source/drain region comprises forming a layer between the first source/drain region and the second source/drain region, having a second conductivity (column 4, line 10).

In re claim 29, Koyama discloses the method of claim, wherein the interposing layer comprises a P+ layer but does not expressly disclose said layer comprising P-. However, using a

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P- layer as an interposing layer would have been obvious to one skilled in the art at the time of the invention for the purpose, for example, of customizing the speed of the charges through the channel region.

In re claim 30, Koyama discloses the method of claim 22, wherein interposing a floating gate structure between the first structure and the gate structure and between the second structure and the gate structure further comprises positioning an insulating layer between the floating gate structure and the first and second columnar structures.

In re claim 31, Koyama discloses the method of claim 30, wherein positioning an insulating layer between the floating gate structure and the first and second columnar structures comprises forming a first insulating layer between the first structure and the floating gate structure having a first thickness and forming a second insulating layer between the second structure and the floating gate structure having a second thickness, the first thickness being less than the second thickness.

In re claim 32, Koyama discloses the method of claim 25, further comprising coupling (shown in Fig. 5) the second source/drain region of the first columnar structure and the second source/drain region of the second columnar structure with a drain line.

5. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kolodny (as above).

In re claim 18, Kolodny discloses the device of claim 13, but does not expressly disclose the empirical measurement of the first distance. It would have been obvious to one having ordinary skill in the art at the time the invention was made to measure the first distance of a very small

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amount, as shown in Fig. 2 of Kolodny, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F. 2c 272, 205 USPQ 215 (CCPA 1980).

#### ***Allowable Subject Matter***

6. Claims 15, 19-21, 23, 24 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Response to Arguments***

7. Applicant's arguments with respect to claims 13 and 16-21 have been considered but are moot in view of the new ground(s) of rejection.

#### ***Conclusion***


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty  
Examiner  
Art Unit 2815

  
**GEORGE ECKERT**  
**PRIMARY EXAMINER**